AMENDMENTS TO THE CLAIMS

Please, add new claims 2-40 as indicated below. All claims pending in this application are reproduced below.

1   1.   (Currently Amended) A computer implemented method of deserializing a data

2   transmission, which is encoded in one communication protocol of a plurality of different

3   communication protocols, comprising the steps of:

4   receiving the data transmission, wherein the data transmission includes a clock

5   portion and a data portion;

6   identifying the communication protocol the data transmission is encoded in;

7   providing a plurality of programmable hardware circuits and programmable

8   software modules to provide a plurality of deserializing functions, the

9   hardware circuits providing deserializing functions that are applicable to a

10   first of the communication protocols, the software modules providing

11   deserializing functions that are applied to a second of communication

12   protocols;

13   determining a first of said programmable hardware circuits and a first of said

14   programmable software modules that are required to deserialize the data

15   transmission according to the ~~determined~~ identified communication

16   protocol;

17   programming said first programmable hardware circuit and first programmable

18   software module with parameters required to deserialize the data

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19   transmission according to the identified communication determined

20   transmission protocol;

21   utilizing said programmed first plurality of programmable hardware circuit and

22   said programmed first programmable software modules to apply a plurality

23   of deserializing functions to deserialize the data transmission according to

24   the identified transmission communication protocol, wherein the

25   deserializing functions include:

26   inverting the polarity of the data transmission if required by the identified

27   communication protocol;

28   detecting a start condition for the data transmission according to the programmed

29   parameters;

30   separating a clock portion and a data portion of the data transmission according to

31   the programmed parameters if required by the identified communication

32   protocol if required by the identified communication protocol;

33   dividing the clock portion by a factor required by the identified communication

34   protocol according to the programmed parameters if required by the

35   identified communication protocol;

36   determining the data integrity of the data transmission according to the

37   programmed parameters if required by the identified communication

38   protocol;

39   detecting an end of packet pattern that signifies the end of the data portion

40   according to the programmed parameters if required by the identified

41   communication protocol;

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42   decoding the data portion of the data transmission according the decoding

43   protocol required by the identified ~~transmission~~ communication protocol;

44   unstuffing bits from the data transmission according to the programmed

45   parameters if required by the identified communication protocol;

46   identifying a synchronization pattern utilized by the ~~determined transmission~~

47   identified communication protocol to determine if the data transmission is

48   being sampled at the correct rate and utilizing the determined

49   synchronization pattern to determine if the data transmission is being

50   sampled at the correct rate if required by the identified communication

51   protocol;

52   storing the decoded data in a data storage medium, which includes a variable size

53   data buffer according to the programmed parameters; and

54   for each of the deserializing functions applied, generating an interrupt and

55   transmitting the interrupt to a CPU.

1   2.   (New) A universal programmable serializer/deserializer for implementing two or

2   more communications protocols in a communications system having a computer

3   processor, the serializer/deserializer comprising:

4   a deserializer coupled to the computer processor for receiving data from a data

5   network and communicating the data to the computer processor and for

6   selectably implementing protocol specific receive functions, the

7   deserializer configured to receive a first program signal indicating a set of

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8   protocol specific characteristics for selecting the protocol specific receive

9   functions; and

10   a serializer for receiving the data from the computer processor and communicating

11   the data to the data network, and for selectably implementing protocol

12   specific transmit functions, the serializer configured to receive a second

13   program signal indicating a set of protocol specific characteristics for

14   selecting the protocol specific transmit functions.

1   3.   (New) The universal programmable serializer/deserializer of claim 2, wherein the

2   protocol specific transmit functions comprise at least one of a shift count function, an idle

3   signal transmission, an End-Of-Packet pattern transmission, and an encoding scheme

4   function.

1   4.   (New) The universal programmable serializer/deserializer of claim 2, wherein the

2   protocol specific receive functions comprise at least one of a polarity inversion, a clock

3   separation, a clock division, a clock frequency selection, a clock phase selection, a start

4   condition detection, a shift bit counting, an End-Of-Packet pattern detection, a

5   synchronization pattern detection, and a decoding scheme function.

1   5.   (New) A deserializer for receiving data transmitted over a network, the

2   deserializer in a universal serializer/deserializer programmable for implementing two or

3   more communications protocols, the deserializer comprising:

4   a programmable receive data circuit for receiving the data, for performing initial

5   data receive functions, and for coupling to a network connection;

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6   a synchronization circuit for selectably detecting a synchronization pattern in the

7   data, the synchronization circuit configured to be programmed with the

8   synchronization pattern corresponding to a current protocol of the two or

9   more communications protocols, and coupled to the programmable receive

10   data circuit for signaling a match signal in response to matching the

11   synchronization pattern with the data;

12   a selectable CRC circuit for detecting errors in the data and determining integrity

13   of the data, the selectable CRC circuit coupled to the programmable

14   receive data circuit for signaling in response to detecting an error in the

15   data;

16   a data storage device for storing the data to be accessed by a CPU, the data storage

17   device coupled to the programmable receive data circuit for receiving the

18   data; and

19   an interrupt generator for generating interrupt signals in response to interrupt

20   generating signals, the interrupt generator coupled to the programmable

21   receive data circuit, the selectable CRC circuit, the synchronization circuit,

22   and the data storage device for receiving the interrupt generating signals,

23   and coupled to the CPU for providing the interrupt signals.

1   6.   (New) The deserializer of claim 5, wherein the protocol specific receive functions

2   comprise at least one of decoding the data according to a decoding scheme, separating

3   clock signals from data signals in the data, inverting polarity of the data signals, and

4   storing the data into a shift register.

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1   7.   (New) The deserializer of claim 6, wherein the decoding scheme is one of

2   Manchester decoding scheme or Non-Return-to-Zero Inverted ("NRZI") decoding

3   scheme.

1   8.   (New) The deserializer of claim 5, wherein the programmable receive data circuit

2   further comprises hardware that enables a receive function required for at least two of the

3   two or more communications protocols.

1   9.   (New) The deserializer of claim 5, wherein the synchronization circuit is not

2   selected in response the current protocol being a UART protocol.

1   10.   (New) The deserializer of claim 5, wherein the synchronization pattern

2   programmed in the synchronization circuit is a logic 00000001 and the current protocol is

3   USB 1.1.

1   11.   (New) The deserializer of claim 5, wherein the selectable CRC circuit is a module

2   implementing a CRC function from software instructions.

1   12.   (New) The deserializer of claim 5, further comprising an End-Of-Packet detector

2   for selectably detecting an End-Of-Packet pattern, the End-Of-Packet detector configured

3   to be programmed with the End-Of-Packet pattern corresponding to the current protocol

4   of the two or more communications protocols, configured to not operate in response to

5   not being selected, and configurable to couple to the network connection for receiving the

6   data and to the interrupt generator for signaling an End-Of-Packet detection.

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1   13.   (New) The deserializer of claim 12, wherein the End-Of-Packet pattern

2   programmed in the End-Of-Packet detector is one of a two single ended zeros and a J-

3   state according to a USB 1.1 protocol and a high pulse held in a range of 62.5 to 600

4   nanoseconds according to a 10-base T protocol.

1   14.   (New) The deserializer of claim 12, wherein the End-Of-Packet detector further

2   comprises:

3   a register for storing the End-Of-Packet pattern programmed in the End-Of-

4   Packet detector; and

5   a comparator coupled to the programmable receive data circuit and the register

6   for comparing the data with the End-Of-Packet pattern.

1   15.   (New) The deserializer of claim 5, wherein the data storage device is one of a

2   programmable data storage unit and a non-programmable double buffer.

1   16.   (New) The deserializer of claim 15, wherein the data storage device is the

2   programmable data storage unit configured to be programmed to modify its data storage

3   capability to meet the requirements of the protocol.

1   17.   (New) The deserializer of claim 5, wherein the data storage device further

2   comprises a set of selectable buffers, the data storage device configured to receive a

3   program signal indicating a bit limit for the current protocol of the two or more

4   communications protocols and coupled to the interrupt generator for providing a signal in

5   response to reaching the bit limit.

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1 18.   (New) The deserializer of claim 17, wherein the data storage device is further

2 configured to select a number of buffers of the set of selectable buffers, the number of

3 buffers corresponding to a number of data bits required to store a bit limit number of bits.

1 19.   (New) A data receive circuit for a deserializer in a universal programmable

2 serializer/deserializer having a synchronization circuit, a data storage device and a CRC

3 circuit for implementing a programmed protocol from a set of communications protocols,

4 the data receive circuit comprising:

5   an exclusive-OR gate (XOR) configurable to be coupled to a network connection

6   for receiving an input signal carrying a data and for selectably performing

7   a polarity inversion of the input signal;

8   a polarity inverter coupled to the XOR for inverting the input signal and

9   configured to receive a first program signal indicating whether the

10   programmed protocol requires the polarity inversion;

11   a clock detection and configuration circuit coupled to the XOR for detecting a

12   protocol specific start condition of the programmed protocol selected from

13   a set of programmed start condition patterns and for providing a protocol

14   specific clock signal of the programmed protocol selected from a set of

15   programmed clock signal definitions in response to receiving a protocol

16   selection indicating the programmed protocol;

17   a clock/data separation circuit coupled to the clock detection and configuration

18   circuit for selectably providing separation of clock information from data

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19   information in the input signal in response to receiving the protocol

20   selection indicating the programmed protocol;

21   a decoder coupled to the clock/data separation circuit for selectably performing a

22   protocol specific decoding function of the programmed protocol selected

23   from a set of programmed decoding functions in response to receiving the

24   protocol selection indicating the programmed protocol;

25   a multiplexer coupled to the clock detection and configuration circuit, to the

26   clock/data separation circuit, and to the decoder for supplying the protocol

27   selection and configured to receive a second program signal indicating the

28   requirements of the programmed protocol;

29   a receive shift register coupled to the decoder, to the synchronization circuit, to

30   the CRC circuit and to the data storage device, the receive shift register for

31   receiving the data one bit at a time from the decoder and providing the

32   data, several bits at a time, to the synchronization circuit, the CRC circuit,

33   and the data storage device;

34   a control logic circuit coupled to the receive shift register, and the synchronization

35   circuit, the control logic for receiving a synchronization match signal from

36   the synchronization circuit and for instructing the receive shift register to

37   provide the data to one of the synchronization device and the data storage

38   device and for setting a number of bits in the several bits used in

39   accordance to the programmed protocol in response to a third program

40   signal indicating the number of bits required by the programmed protocol.

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1 20. (New) The data receive circuit of claim 19, wherein the first program signal is a

2 bit of a protocol selection word.

1 21. (New) The data receive circuit of claim 19, wherein the set of programmed start

2 condition patterns programmed in the clock detection and configuration circuit comprises

3 an Inter-Integrated-Circuits ("I^{2}C") falling edge with a high clock, a UART falling edge, a

4 SPI rising clock edge.

1 22. (New) The data receive circuit of claim 19, wherein the clock detection and

2 configuration circuit further comprises:

3 a clock sampler having an edge detector coupled to the XOR for sampling the

4. clock to detect the rising and falling edges of the input signal in detecting

5 the protocol specific start condition of the programmed protocol; and

6 a phase lock loop for generating a clock signal with a programmable frequency

7 and a programmable phase in providing the protocol specific clock signal

8 of the programmed protocol;

1 23. (New) The data receive circuit of claim 19, wherein the multiplexer bypasses one

2 or more of the clock detection and configuration circuit, the clock/data separation circuit,

3 and the decoder in response to the second program signal indicating the programmed

4 protocol requirements.

1 24. (New) The data receive circuit of claim 19, wherein the clock/data separation

2 circuit further selectably provides clock division of the clock signal as required by the

3 programmed protocol.

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1 25. (New) The data receive circuit of claim 19, wherein the set of programmed

2 decoding functions of the decoder comprises a function from the group consisting of a

3 Non-Return-to-Zero Inverted ("NRZI") decoding function and a Manchester decoding

4 function.

1 26. (New) The data receive circuit of claim 25, wherein the function from the group

2 consisting of a Non-Return-to-Zero Inverted ("NRZI") decoding function and a

3 Manchester decoding function of the decoder are programmed in a hardware

4 implementation for being performed faster than decoding functions programmed in a

5 software implementation.

1 27. (New) The data receive circuit of claim 19, wherein the decoder further selectably

2 performs bit unstuffing in response to being required by the programmed protocol.

1 28. (New) The data receive circuit of claim 19, wherein the control logic circuit is

2 further coupled to a shift count register indicating a number of bits loaded into the receive

3 shift register.

1 29. (New) The data receive circuit of claim 28, wherein the number of bits loaded into

2 the receive shift register is used in response to the programmed protocol not having a fix

3 number of bits.

1 30. (New) A synchronization circuit for a deserializer in a universal programmable

2 serializer/deserializer having a data receive circuit, the serializer/deserializer for

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3   implementing a programmed protocol from a set of communications protocols, the

4   synchronization circuit comprising:

5   a synchronization register configured to receive a first program signal indicating a

6   synchronization pattern corresponding to the programmed protocol;

7   a programmable synchronization mask coupled to the synchronization register

8   through as set of logic gates for masking out a corrupted bit for optimizing

9   the synchronization circuit to operate in a particular environment, the

10   programmable synchronization mask configured to receive a program

11   signal indicating settings for the masking; and

12   a comparator coupled to the programmable receive data circuit for receiving an

13   input data signal and coupled to the logic gates for receiving the

14   synchronization pattern, the comparator for comparing the synchronization

15   pattern with the input data signal and for producing a match signal in

16   response to matching the synchronization pattern with the input data

17   signal.

1   31.   (New) The data receive circuit of claim 30, wherein the logic gates are AND gates

2   which modify the corrupted bit by changing a logic value of the corrupted bit to a

3   programmed logic value indicated by the settings.

1   32.   (New) The data receive circuit of claim 30, wherein the comparator is a digital

2   comparator.

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1   33.   (New) A serializer for transmitting data over a network, the serializer in a

2   universal serializer/deserializer programmable for implementing two or more

3   communications protocols, the serializer comprising:

4   a data buffer for receiving the data to be transmitted from a processor and

5   configured to receive a load signal for loading off the data;

6   a transmit shift register coupled to the data buffer for loading the data off the data

7   buffer, the shift register further for serially shifting the data out;

8   a control logic circuit coupled to the data buffer for providing the load signal and

9   configured to receive a bit number corresponding the a current protocol of

10   the two or more communications protocols, wherein the load signal is

11   provided upon reaching a bit-number number of bits received by the data

12   buffer; and

13   a programmable encoder coupled to the transmit shift register for receiving the

14   shifted out data, for selectably performing an encoding function required

15   for the current protocol in response to receiving a protocol selection signal

16   indicating the current protocol, and for transmitting the data out of the

17   serializer.

1   34.   (New) The serializer of claim 33, wherein the control logic circuit further

2   comprises a shift counter configured to receive a program signal indicating the bit number

3   and configured to count a number of bits received by the data buffer and to indicate the

4   number of bit reaching the bit-number.

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1   35.   (New) The serializer of claim 33, further comprising an End-Of-Packet generator

2   coupled to the control logic circuit and to the programmable encoder for selectably

3   generating a End-Of-Packet pattern corresponding to the current protocol in response to

4   receiving a last bit signal from the control logic circuit and for providing the End-Of-

5   Packet pattern to the programmable encoder for transmission.

1   36.   (New) The serializer of claim 33, further comprising a programmable idle circuit

2   for selectably providing an idle signal corresponding to the current protocol in response to

3   the transmit shift register having no data to transmit.

1   37.   (New) The serializer of claim 36, wherein the idle signal is one of an all logic zero

2   state, an all logic one state, and a tri-state.

1   38   (New) A method of communicating data in a data network according to a protocol

2   selected from a set of protocols using a universal programmable serializer/deserializer,

3   the method comprising the steps of:

4   determining the protocol from the set of protocols to be implemented for

5   communicating in the data network;

6   providing a set of program signals to the universal programmable

7   serializer/deserializer indicating a set of protocol specific functions

8   required to communicate using the protocol;

9   determining whether data is being received by the universal programmable

10   serializer/deserializer;

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11   receiving a receive data interrupt from the universal programmable

12   serializer/deserializer; and

13   in response to receiving the receive data interrupt reading data into a processor.

1   39   (New).A protocol translation system for protocol conversion between networks

2   operating under different communication protocols, the protocol translation system

3   comprising:

4   a first universal programmable serializer/deserializer for receiving data from a

5   first network operating under a first protocol and for implementing the

6   first protocol to remove protocol specific information to output a data

7   payload, the first serializer/deserializer configured to receive a first set of

8   program signals indicating a first set of requirements of the first protocol;

9   and

10   a second universal programmable serializer/deserializer coupled to the first

11   serializer/deserializer for receiving the payload data from the first

12   serializer/deserializer and for transmitting to a second network operating

13   under a second protocol and for implementing the second protocol to

14   introduce protocol specific information to the data payload, the second

15   serializer/deserializer configured to receive a second set of program

16   signals indicating a second set of requirements of the second protocol.

1   40.   (New) The protocol translation system of claim 39, wherein the first protocol is a

2   USB protocol and the second protocol is a 10-baseT protocol.

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